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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,475	05/11/2001	James E. Justiss	200265	6670

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OSTRAGER CHONG FLAHERTY & BROITMAN PC
250 PARK AVENUE, SUITE 825
NEW YORK, NY 10177

EXAMINER	
MEHRPOUR, NAGHMEH	

ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/853,475	JUSTISS ET AL.	
	Examiner	Art Unit	
	Naghmeh Mehrpour	2686	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida et al. (US Patent 5,860,057).

Regarding claim 1, Ishida teaches a method of digitally canceling interference on a received signal comprising adaptively canceling interference on the received signal using an interference reference feedback signal, the feedback signal acquired downstream from a digital processor (col 8 lines 32-57).

Regarding claim 2, Ishida teaches a method further comprising subtracting an counter-interference signal from the received signal to form a desired signal (col 7 lines 40-41).

Regarding claim 3, Ishida teaches a method further comprising digitally processing said desired signal to generate said feed back interference reference signal (col 8 lines 31-57).

Regarding claim 4, Ishida teaches a method further comprising correlating said interference reference feedback signal to said desired signal to generate an error signal (col 8 lines 25-31).

Regarding claim 5, Ishida teaches a method wherein adaptively canceling interference on the received signal farther comprising generating said counter-interference signal based on said error signal to cancel said interference (col 8 lines 63-67, col 9 lines 1-29).

Regarding claim 6, Ishida teaches a method wherein adaptively canceling interference further comprises iteratively canceling interference on the received signal until said error signal equals zero (col 9 lines 15-67, col 10 lines 1-20).

Regarding claim 7, Ishida teaches a method wherein said adaptively canceling interference farther comprises digitally and accurately replicating the interference (col 5 lines 40-67, col 6 lines 1-45).

Regarding claim 8, Ishida teaches a method further comprising simultaneously digitally canceling interference on a plurality of received signals (col 3 lines 5 lines 40-67, col 6 lines 1-45).

Regarding claim 9, Ishida teaches a method further comprising sequentially digitally canceling interference on a plurality of received signals (col 3 lines 40-67, col 6 lines 1-45).

Regarding claim 10, Ishida teaches a method of canceling interference within the satellite payload (col 5 lines 1-67, col 6 lines 1-2) comprising:

receiving a communication signal having interference (col 6 lines 9-45);

converting said communication signal into the received signal (col 7 lines 10-39);

a subtract or subtracting a counter-interference signal from the received signal to form a desired signal (col 7 lines 40-50);

a correlator correlating said interference reference feedback signal to said desired signal to generate an error signal (col 8 lines 26-67, col 0032);

adaptively canceling interference on the received signal based on said error signal by generating said counter-interference signal to cancel said interference (col 9 lines 16-67, col 10 lines 1-20).

Regarding claim 11, Ishida teaches a satellite communication system (see figure 1) comprising:

a first antenna for receiving a communication signal (col 9 lines 29-65);

an analog-to-digital converter (ADC) electrically coupled to said first antenna, said ADC converting said communication signal to a received signal (col 9 lines 15-56);

a satellite payload circuit comprising a first input, a second input, and an output, said first input is electrically coupled to said ADC (col 9 lines 16-67, col 10 lines 1-6);

said satellite payload circuit digitally processing said received signal to form an interference reference feedback signal (col 9 lines 15-67, col 10 lines 1-6);

a feedback signal path electrically coupling said output to said second input said feedback signal path transferring said interference reference feedback signal from said output to said second input (col 9 lines 15-67, col 10 lines 1-20).

Regarding claim 12, Ishida teaches a system wherein said communication circuit (see figure 1,0024) comprises:

a subtractor electrically coupled to said ADC, said subtractor subtracting a counter-interference signal from said received signal to form a desired signal (col 9 lines 15-67, col 10 lines 1-20);

a digital processor electrically coupled to said subtractor, said digital processor generating said interference reference feed back signal from said desired signal (col 10 lines 21-67, col 11 lines 1-20);

a correlator electrically coupled to a subtractor (0026, 0030-0031), said correlator comparing a interference reference feedback signal to said desired signal to generate an error signal (col 11 lines 5-67, col 12 lines 1-15); and

a controller electrically coupled to said correlator and said subtractor (col 10 lines 15-67, col 10 lines 1-20);

said controller adaptively canceling interference on said received signal based on said error signal (col 9 lines 15-67, col 10 lines 1-20).

Regarding claim 13, Ishida teaches a communication system comprising:

a first antenna for receiving a communication signal (col 6 lines 48-67, col 7 lines 1-10);

an analog-to-digital converter (ADC) electrically coupled to said first antenna, said ADC converting said communication signal to a received signal (col 6 lines 49-67, col 7 lines 1-10);

a subtractor electrically coupled to said ADC (col 7 lines 40-50), said

subtractor subtracting a counter-interference signal from said received signal to form a desired signal (col 7 lines 40-50);

a digital processor electrically coupled to said subtractor, said digital processor generating said interference reference feed back signal from said desired signal (col 6 lines 46-67, col 7 lines 1-39);

a correlator electrically coupled to said summing junction, said correlator comparing said interference reference signal to said desired signal to generate an error signal (col 6 lines 46-67, col 7 lines 1-39); and

a controller electrically coupled to said substractor and said controller adaptively canceling interference on said received signal based on said error signal (col 7 lines 40-67 col 8 lines 1-23).

Regarding claim 14, Ishida teaches a method of digitally canceling interference on a received signal within a satellite payload comprising adaptively canceling interference on the received signal using an interference reference feedback signal and not using a non-feedback interference signal (col 6 lines 46-67 col 7 lines 1-10).

Response to Arguments

3. Applicant's arguments with respect to claims 1-14, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **Any responses to this action should be mailed to:**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naghmeh Mehrpour whose telephone number is 571-272-7913. The examiner can normally be reached on 8:00- 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha Banks-Harold be reached (571) 272-7905.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NM

March 31, 2006